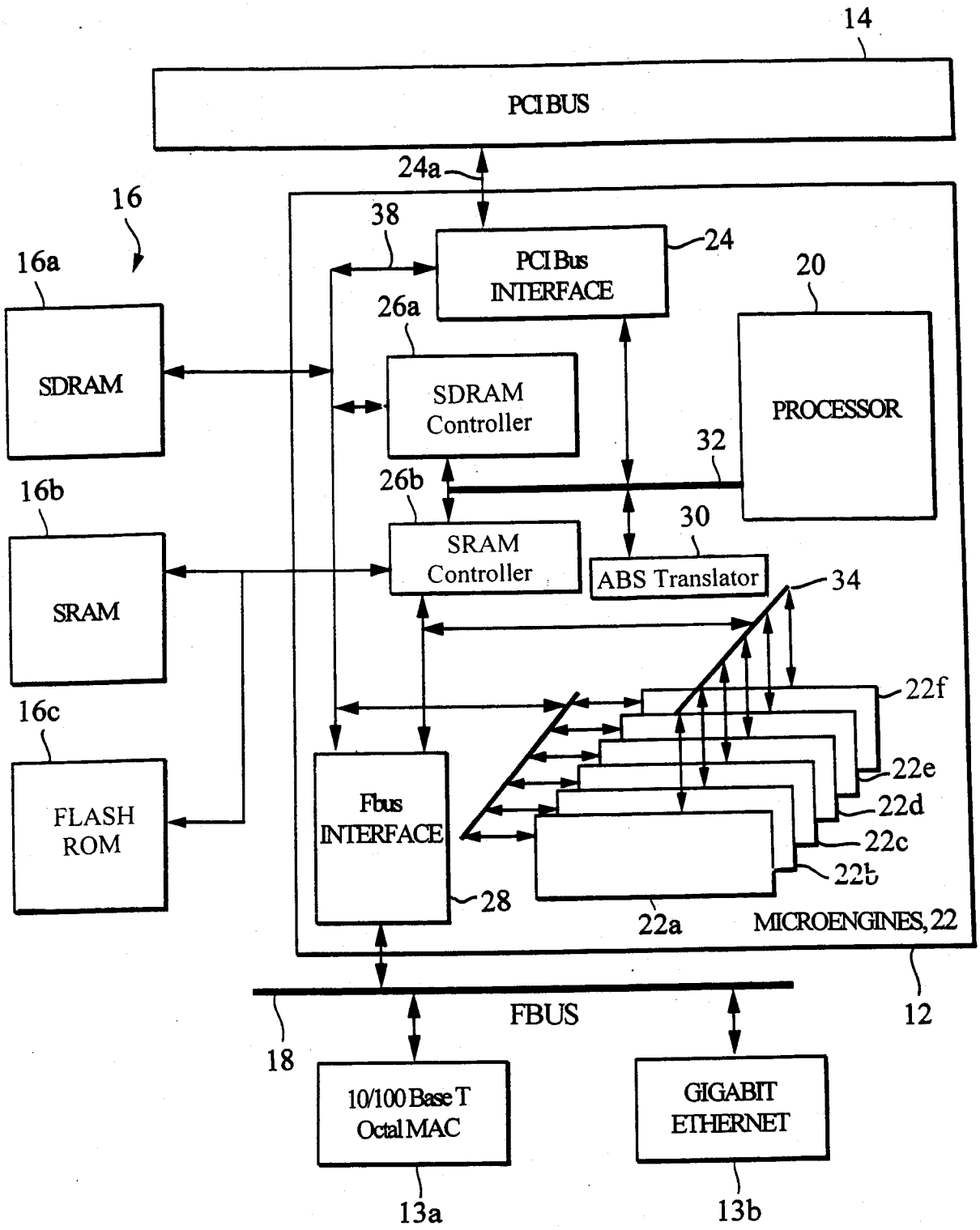

14
PCI BUS
24a
16
38
16a
PCI Bus INTERFACE
24
20
26a
SDRAM
SDRAM Controller
PROCESSOR
32
16b
26b
30
SRAM
SRAM Controller
ABS Translator
34
22f
16c
22e
22d
FLASH ROM
Fbus INTERFACE
22c
22b
28
22a
MICROENGINES, 22
FBUS
12
18
10/100 Base T Octal MAC
GIGABIT ETHERNET
13a
13b

FIG. 1

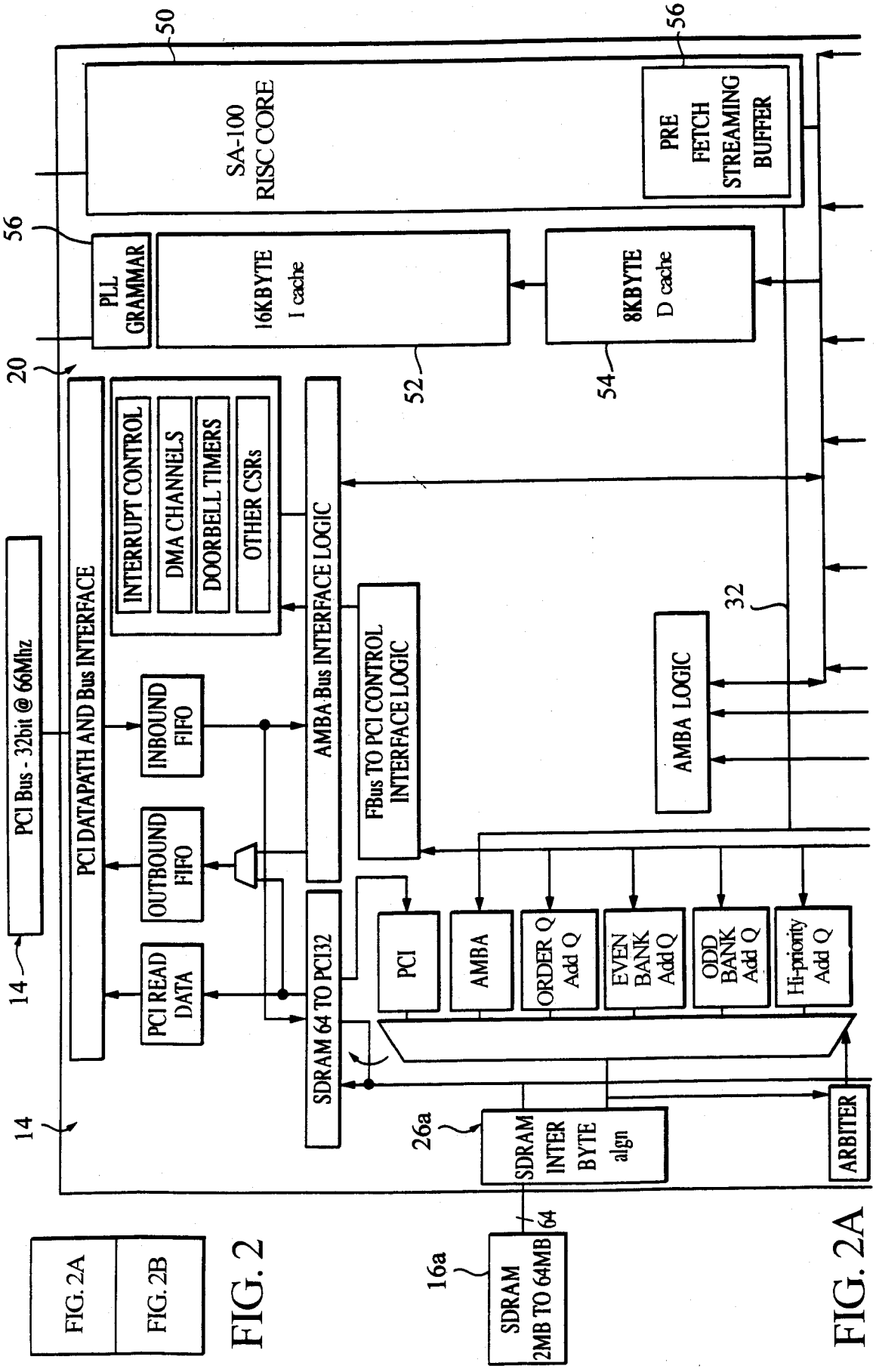


FIG. 2A

FIG. 2A
FIG. 2B

FIG. 2

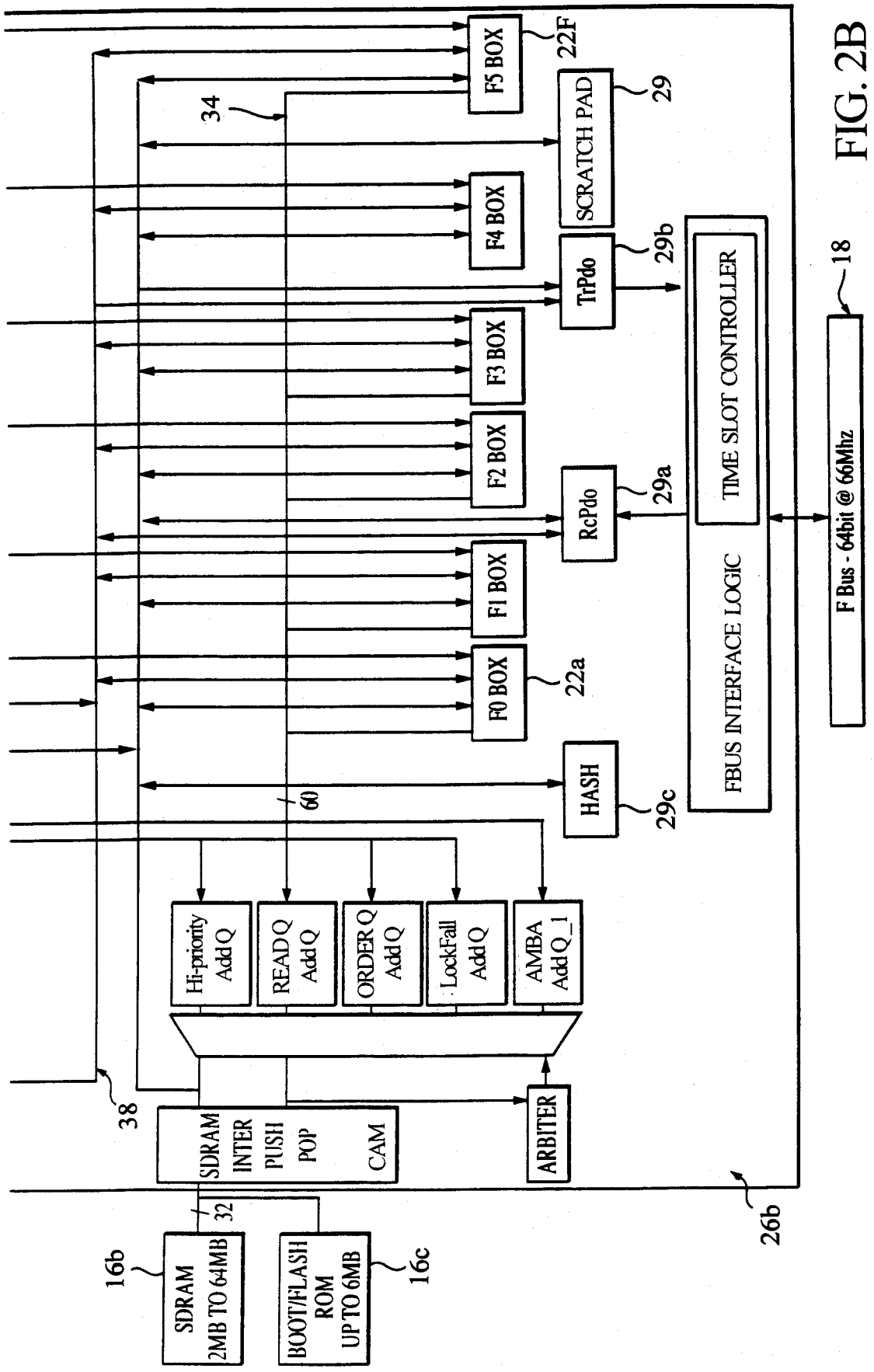

F5 BOX
22F
34
SCRATCH PAD
29
F4 BOX
TrPdo
29b
TIME SLOT CONTROLLER
18
F3 BOX
F2 BOX
RcPdo
29a
F1 BOX
F0 BOX
22a
F Bus - 64bit @ 66Mhz
HASH
29c
FBUS INTERFACE LOGIC
60
Hi-priority Add Q
READ Q Add Q
ORDER Q Add Q
LockFail Add Q
AMBA Add Q_1
38
SDRAM INTER PUSH POP CAM
ARBITER
32
26b
16b
SDRAM 2MB TO 64MB
BOOT/FLASH ROM UP TO 6MB
16c

FIG. 2B

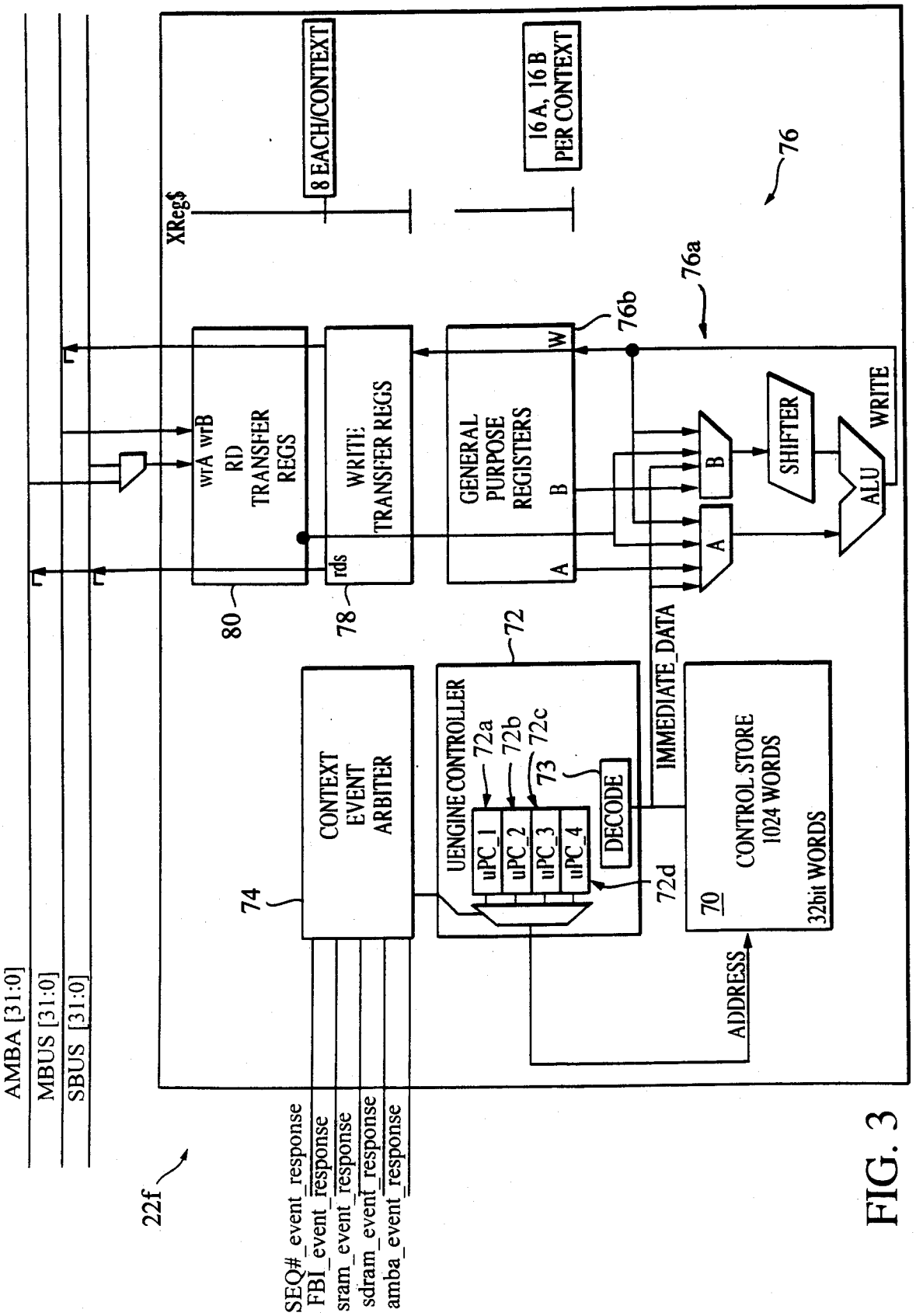

AMBA [31:0]
MBUS [31:0]
SBUS [31:0]
22f
SEQ#_event_response
FBI_event_response
sram_event_response
sdram_event_response
amba_event_response
XReg$
8 EACH/CONTEXT
16 A, 16 B PER CONTEXT
76
76a
76b
wrA wrB
RD TRANSFER REGS
WRITE TRANSFER REGS
GENERAL PURPOSE REGISTERS
W
B
A
rds
80
78
SHIFTER
ALU
WRITE
72
UENGINE CONTROLLER
72a
72b
72c
73
uPC_1
uPC_2
uPC_3
uPC_4
DECODE
72d
IMMEDIATE_DATA
CONTEXT EVENT ARBITER
74
CONTROL STORE 1024 WORDS
32bit WORDS
70
ADDRESS

FIG. 3

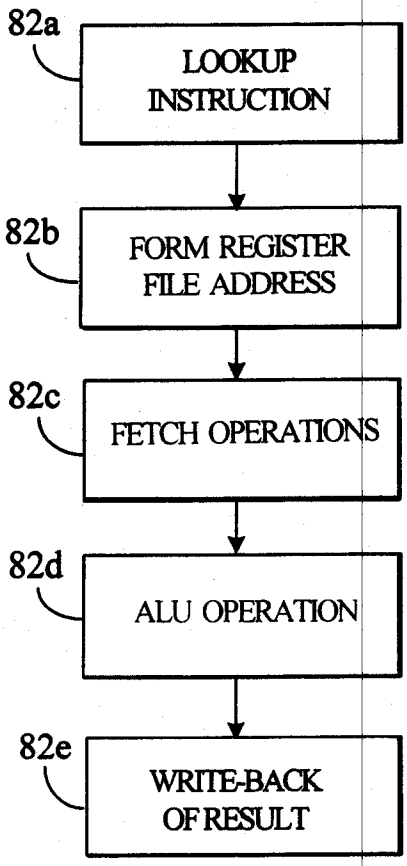
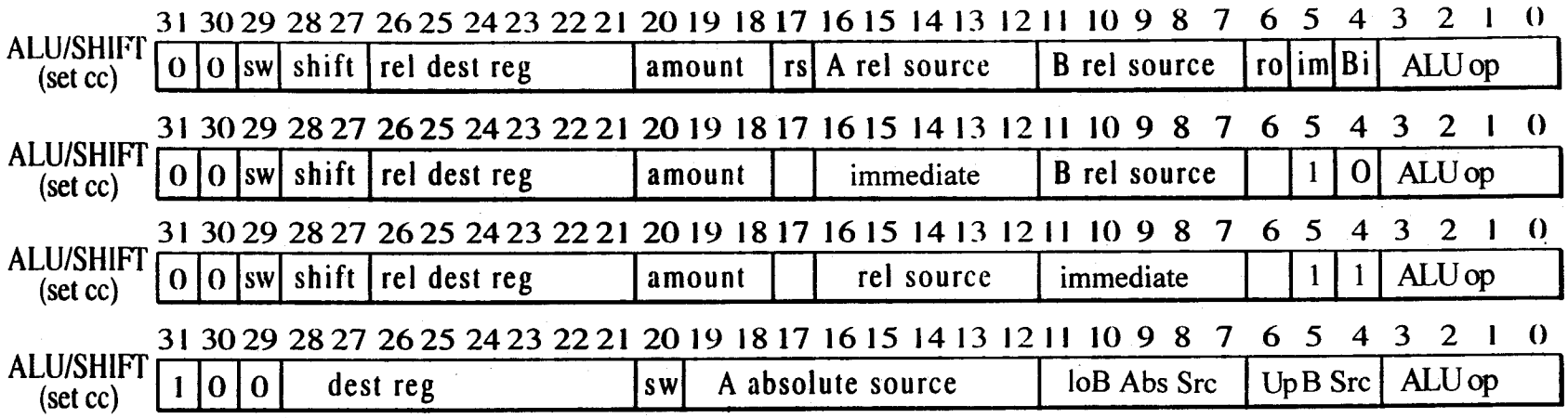

82a
LOOKUP INSTRUCTION
82b
FORM REGISTER FILE ADDRESS
82c
FETCH OPERATIONS
82d
ALU OPERATION
82e
WRITE-BACK OF RESULT

FIG. 4



Shift Decode:

(rs,r0) decode ([31:0] shifts into [63:32] and take [63:32]):

00 = left rotate

01 = right shift (32-ShfAmt = Right Shift Amt)

10 = left shift

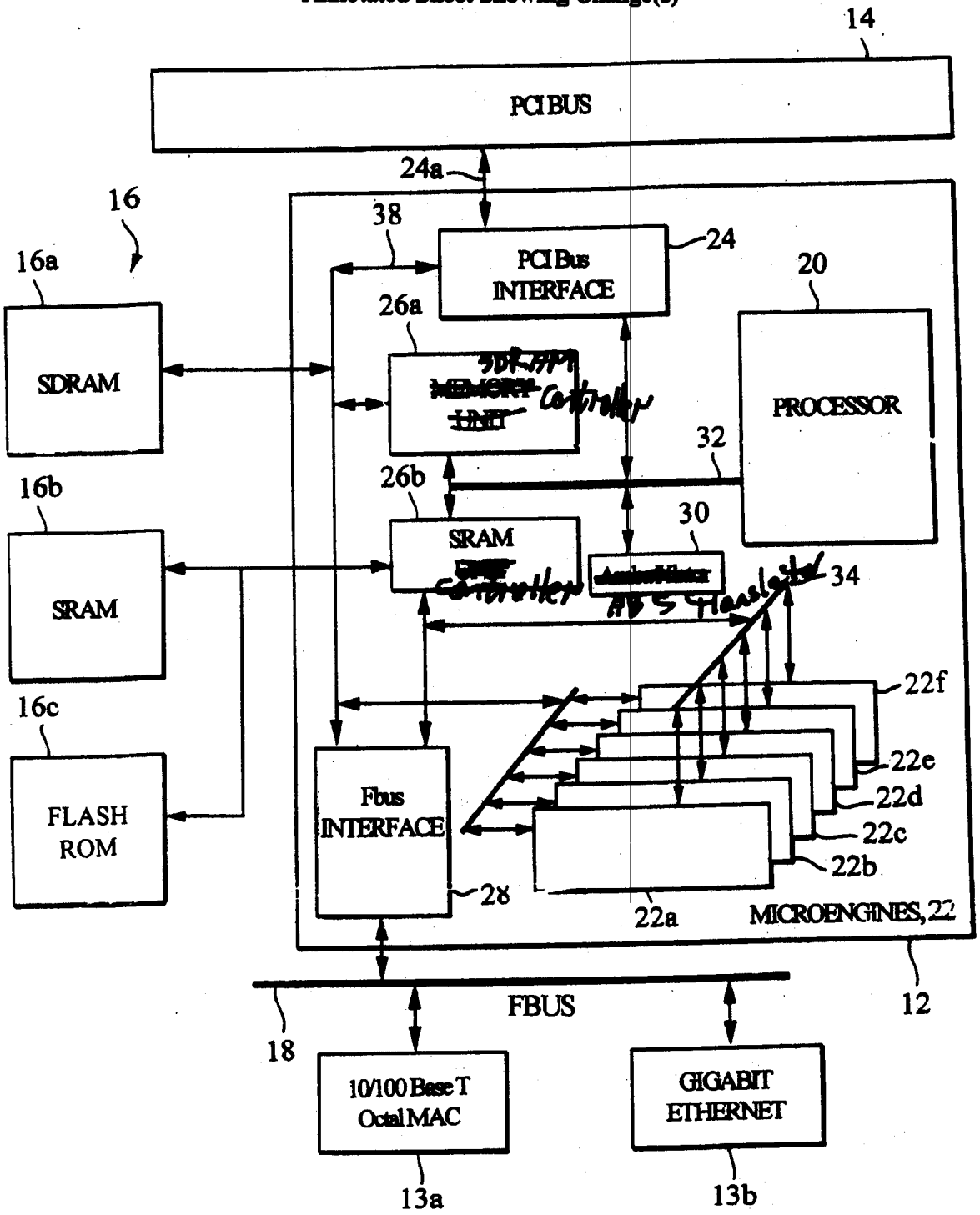
11= double shift (upper A-op shifts into lower B-op)

===> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B	0100 = ~A&B (~and)	1000 = A-B	1100 = A+B(8)
0001 = ~B	0101 =XOR	1001 = B-A	1101 = A+B(16)
0010 = A&B (and)	0110 = OR	1010 =	1110 = A+B
0011= A&~B (and~)	0111= mul-stuff	1011=	1111= A+B+Cin

FIG. 5


14
PCI BUS
24a
16
38
16a
PCI Bus INTERFACE
24
20
26a
SDRAM
PROCESSOR
32
16b
26b
30
SRAM
SRAM
34
16c
22f
22e
22d
22c
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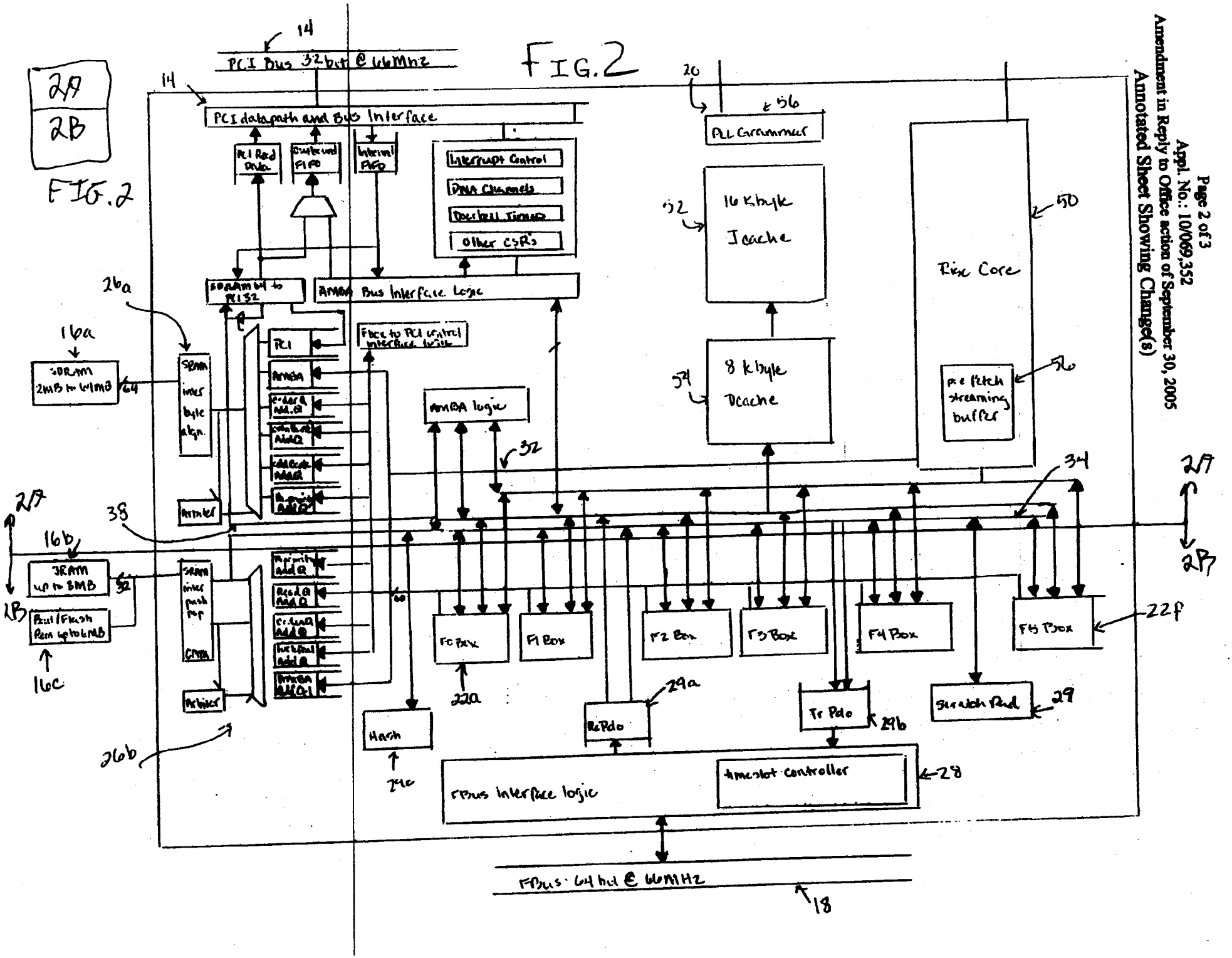
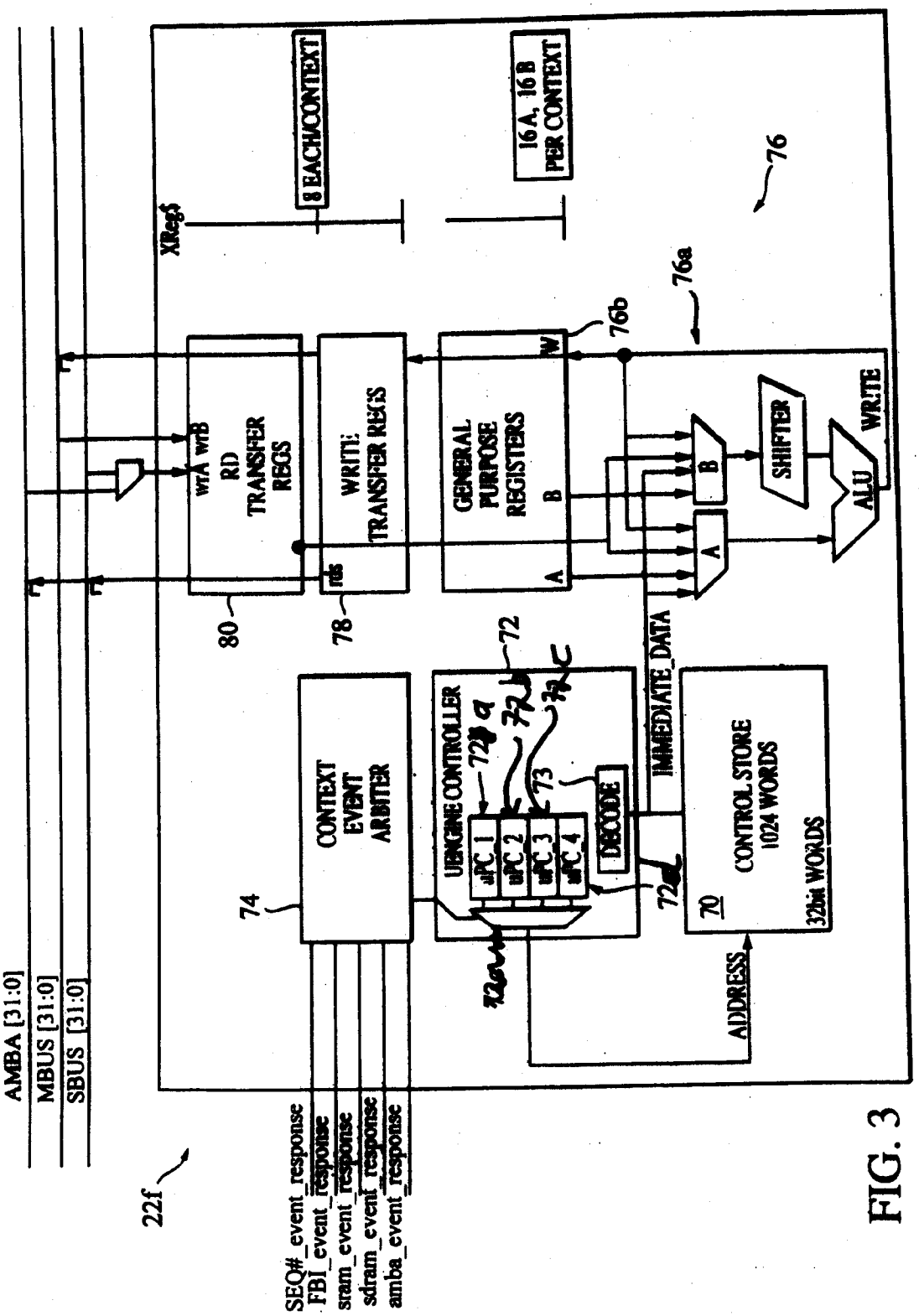
FLASH ROM
Fbus INTERFACE
28
22a
MICROENGINES, 22
FBUS
18
12
10/100 Base T Octal MAC
GIGABIT ETHERNET
13a
13b

FIG. 1

FIG. 2


14
PCI Bus 32 bit @ 66MHz
PCI datapath and Bus Interface
PCI Read Data
Internal FIFO
Interrupt Control
DMA Channels
Other CSRs
20
PLL Generator
16 Kbyte Icache
Risc Core
8 kbyte Dcache
pre fetch streaming buffer
SDRAM to PCI32
AMBA Bus Interface Logic
Risc to PCI control interface bridge
PCI
AMBA
AMBA logic
SDRAM 2MB to 64MB
SDRAM interface byte align
Arbiter
SDRAM interface push pop
SDRAM up to 8MB
Flash/Flash Rom up to 4MB
FC Box
F1 Box
F2 Box
F3 Box
F4 Box
F5 Box
Hash
RcPdo
Tr Pdo
Scratch Pad
Fbus interface logic
timeslot controller
Fbus: 64 bit @ 66MHz
18
26a
26b
16a
16b
16c
22a
22f
24a
28
29
29a
29b
32
34
38
50
52
54
56


AMBA [31:0]
MBUS [31:0]
SBUS [31:0]
22f
8 EACH/CONTEXT
16 A, 16 B PER CONTEXT
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76a
76b
XReg's
RD TRANSFER REGS
WRITE TRANSFER REGS
GENERAL PURPOSE REGISTERS
SHIFTER
ALU
WRITE
80
78
72
CONTEXT EVENT ARBITER
UENGINE CONTROLLER
DECODE
IMMEDIATE_DATA
CONTROL STORE 1024 WORDS
32bit WORDS
74
70
ADDRESS
SEQ# event_response
FBI_event_response
sram_event_response
sdram_event_response
amba_event_response

FIG. 3